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E.D.

5/8/03

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/332,277
Filing Date June 11, 1999
Inventor Klaus Florian Schuegraf et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Ron E. Pompey
Attorney's Docket No. MI22-532
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
and Wordline, Transistor Gate, and Conductive Interconnect Structures

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

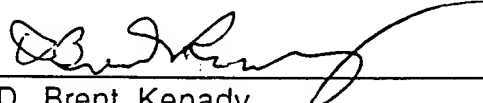
References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether any of the submitted references is prior art. Copies of the references are attached.

Respectfully Submitted:

Dated: _____

5-6-02


D. Brent Kenady
Reg. No. 40,045

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/332,271
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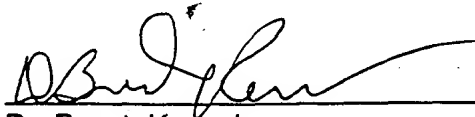
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

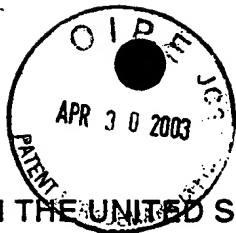
The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether any of the submitted references is prior art. Copies of the references are attached.

Respectfully Submitted:

Dated: 3-13-02


D. Brent Kenady
Reg. No. 40,045

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EL 844055557 US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/322,271
Filing Date June 11, 1999
Inventor Klaus Florian Schuegraf et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Ron E. Pompey
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with
37 CFR §1.56. No admission is made regarding whether any of the submitted
references is prior art. Copies of the references are attached.

Respectfully Submitted:

Dated: 2-7-02


D. Brent Kenady
Reg. No. 40,045

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EL 355818248



Inventor: Klaus Florian Schuegraf et al.
Title: Methods For Forming Wordlines, Transistor Gates, And Conductive
Interconnects, And Wordline, Transistor Gate, and Conductive
Interconnect Structures
Assignee: Micron Technology, Inc.

INFORMATION DISCLOSURE STATEMENT

The Examiner's attention is directed to the references listed on the attached
Form PTO-1449 and copies of which are attached.

Citation of these references are respectfully requested.

Respectfully submitted,

Date: 6/11/99

Attorney: David G. Latwesen
David G. Latwesen, Ph.D.
Reg. No. 38,533

Date: _____

Inventor: _____
Klaus Florian Schuegraf

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Date: 5/24/99

Inventor: Randhir P. S. Thakur
Randhir P. S. Thakur